Workshop on 1st JILP Data Prefetching Championship

http://www.jilp.org/dpc/

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About DPC-1

• Goals
  – Encourage architects to think more about data prefetching
  – Find out best prefetching algorithms
  – Implementation and papers available online

• Contestants invited to submit prefetcher implementations on a common simulation framework

• Top prefetchers based on performance and quality selected for publication
DPC-1 Summary

- 13 papers
  - Papers from three continents! (N. America, Europe, and Asia)
- 20 code submissions
  - Some papers had two or three different variations on the same techniques
- Program Committee selected eight submissions based on performance and quality
- Performance results announced at the end of this workshop
Acknowledgments

• Contestants
• Our Sponsors

• DPC-1 Organizing Committee (Intel)

Alaa Alameldeen (Chair)
Zeshan Chishti
Aamer Jaleel
Daniel Luchi
Chris Wilkerson

• DPC-1 Program Committee

Eric Rotenberg, NC State Univ. (Chair)
Alaa Alameldeen, Intel
Yuan Chou, Sun Microsystems
David Kaeli, Northeastern Univ.
Alvin Lebeck, Duke Univ.
Kyle Nesbit, Google
Suleyman Sair, Intel
Competition Rules

• Implement L1 and L2 prefetching using at most 32kbit of state
  – No limit on logic or hardware complexity otherwise
  – Also provided a “Prefetch” status bit associated with each cache line

• Each contestant limited to 3 submissions
  – Three different techniques
  – Three variations on the same technique
  – Two variations on one technique plus a different technique
Classes of Submitted Prefetchers

• L1 Prefetchers
  – Sequential, next N-blocks
  – PC stride-based
  – Data address stride-based
  – Stream Prefetching

• L2 Prefetchers
  – Sequential
  – PC Stride-based
  – Data address stride-based
  – Region (Czone) –based, with stride or other deltas within a region
  – Combine local and global histories (similar to BP)